herewith.

IN THE CLAIMS:

Please cancel claim 6 in its entirety without prejudice nor disclaimer of the subject matter recited therein.

Please amend claims 1, 3-5 and 7 as follows. Attached hereto is a marked-up copy of the amended claims.

A'
figs. 1, 4

1. (Amended) A high-voltage MOS transistor wherein a resistance value of a source region is set independently of a resistance value of a drain region in such a manner as to maintain a high sustaining breakdown voltage of the transistor, which is based on a voltage of a source offset region and a voltage of a substrate region directly under a gate insulating film during operation of the high-voltage MOS transistor.

figs. 1, 4
A2

3. (Amended) The transistor of Claim 2, wherein the resistance value of the source offset region is set higher than the resistance value of the drain offset region.

fig. 1

4 (Amended) The transistor of Claim 2, wherein a length of the source offset region is set longer than a length of the drain offset region.

Cont. A2 Sub B1

5. (Amended) The transistor of Claim 2, wherein a dopant concentration of the source offset region is set lower than a dopant concentration of the drain offset region.

A3

7. (Amended) The transistor of Claim 1, wherein the resistance value of the source region is set higher than that of the drain region such that the voltage of the substrate region directly under the gate insulating film VW minus a forward biased breakdown voltage of silicon does not exceed a source voltage VS easily, during operation of the high-voltage MOS transistor.